IN THE CLAIMS:

Please amend Claim 1 as shown below. The claims, as currently pending in the application, read as follows:

1. (Currently Amended) A processor system comprising:

a single semiconductor substrate on which is provided a built-in processor, a memory controller, an external bus interface to which an external processor is connected from outside of the single semiconductor substrate, a processor bus which is connected with the built-in processor and the external bus interface, and a cross-bar switch that mutually connects the memory controller and the processor bus,

wherein the cross-bar switch comprises at least a first ~~port~~ interface connected to the memory controller and a second ~~port~~ interface connected to the processor bus,

wherein first and second signal lines for inputting first and second enable signals are connected to reset signal lines of the built-in processor and the external bus interface, respectively, and

wherein the first enable signal is asserted while the second enable signal is deasserted, so that the built-in processor is in a reset state to suppress issuance of a request for using the processor bus from the built-in processor and the external processor connected to the external bus interface can use the processor bus and the second ~~port~~ interface of the cross-bar switch exclusively,

and wherein the second enable signal is asserted while the first enable signal is deasserted, so that the external bus interface is in a reset state to suppress issuance of a

request for using the processor bus from the external processor connected to the external bus interface and the built-in processor can use the processor bus and the second ~~port~~ interface of the cross-bar switch exclusively, without stopping an operation of the external processor.

2. and 3. (Cancelled).

4. (Previously Presented) The processor system according to claim 1, further comprising:

a second built-in processor connected to the cross-bar switch on the semiconductor substrate.

5. and 6. (Cancelled)

7. (Previously Presented) The processor system according to claim 1, wherein the built-in processor and the external bus interface are connected through a bus common to the cross-bar switch.

8. (Previously Presented) The processor system according to claim 1, wherein the built-in processor and the external processor use in common programs stored in a memory controlled by the memory controller.

9. (Previously Presented) The processor system according to claim 1,

further comprising:

an image data transfer bus connected with the cross-bar switch; and

an image output device interface or an image input device interface connected with the image data transfer bus on the semiconductor substrate.